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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/724,164

12/01/2003

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Q78699

9393

23373 7590 09/21/2007
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EXAMINER

SAVLA, ARPAN P

ART UNIT

PAPER NUMBER

2185

MAIL DATE

DELIVERY MODE

09/21/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/724,164

Applicant(s)

HIROSE, YUKITOSHI

Examiner

Arpan P. Savla

Art Unit

2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 August 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 7, 2007 has been entered.

Response to Amendment

This Office action is in response to Applicant's communication filed August 7, 2007 in response to the Office action dated May 7, 2007. Claims 1, 2, and 5 have been amended. Claims 21-38 have been cancelled. Claims 1-20 are pending in this application.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

1. In view of Applicant's amendment, the 112, first paragraph rejection to **claim 1** has been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claim 1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's "Description of the Prior Art" appearing in Applicant's specification, (hereinafter "Applicant's admitted prior art (AAPA)") in view of Chow et al. (U.S. Patent Application Publication 2002/0069317) (hereinafter "Chow") and Thörnblad (U.S. Patent 5,859,545).

4. **As per claim 1**, AAPA discloses a memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data (pg. 2, lines 14-17; Fig. 2), elements 112₁₋₄);

a control device for, in replacing an arbitrary memory module, switching a ring bus from a unidirectional bus capable of either sending or receiving a signal unidirectionally to a bi-directional bus capable of sending and receiving a signal bi-directionally (pg. 2, line 25 – pg. 3, line 5; Fig. 2, element 113); *See the 112 rejection for claim 1 above. It should be noted that "memory controller" is analogous to "control device."* It should also be noted as disclosed in AAPA that the ring bus consists of two unidirectional buses that provide unidirectional functionality when used separately as

well as bi-directional functionality when used together. Thus, when signals are only being sent in one direction, the ring bus is capable of either sending or receiving a signal unidirectionally. However, at some point later when signals are being sent in both directions the ring bus switches to a bus capable of sending and receiving signals bi-directionally.

a CPU which controls said control device for access operation to said memory modules (Fig. 2, element 111),

wherein said buffer sections are connected in series to form a ring bus with said control device, each having a buffer circuit for causing said bus to operate as said unidirectional bus or said bi-directional bus in accordance with an instruction from said control device (pg. 2, lines 14-17; pg. 2, line 21 – pg. 3, line 5; Fig. 2).

AAPA admitted prior art does not expressly disclose a hard disk device to which the data stored in said memory modules is copied;

a control device for detecting an address space of said memory module to be replaced, and accessing a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module to be replaced is requested;

and wherein said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus;

a second buffer circuit for sending a signal to one input/output end of the ring bus;

a third buffer circuit for receiving a signal from the other input/output end of the ring bus;

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus.

Chow discloses a hard disk device to which the data stored in said memory modules is copied (paragraph 135; Fig. 14, elements 110, 130, and 425); *It should be noted that "non-volatile storage module" is analogous to "hard disk device" and "memory matrix module" is analogous to "memory module."*

a control device for detecting an address space of said memory module to be replaced, and accessing a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module to be replaced is requested (paragraph 0168; Fig. 14, element 125). *It should be noted that "management module" is analogous to "control device." It should also be noted that in order for the failover process to be completely transparent to the data processing system it is inherently required the management module detect a memory space in the failed memory matrix module and subsequently access a memory area in the non-volatile storage module corresponding to the detected address space when an access to the memory matrix module that failed is requested.*

AAPA and Chow are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Chow's non-volatile storage module and management module within AAPA's RAMLINK memory system.

The motivation for doing so would have been to minimize delay when the memory matrix failed by providing failover to a backup memory that is completely transparent to a user of the data processing system (Chow, paragraph 0168).

The combination of AAPA/Chow does not expressly disclose said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus;

a second buffer circuit for sending a signal to one input/output end of the ring bus;

a third buffer circuit for receiving a signal from the other input/output end of the ring bus;

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus.

Thörnblad discloses a first buffer circuit for receiving a signal from one input/output end of a bus (col. 3, lines 46-52; Fig. 4, the element corresponding to C1 in Fig. 3); *It should be noted that comparator C1 is analogous to the first buffer circuit.*

a second buffer circuit for sending a signal to one input/output end of the ring bus (col. 3, lines 46-52; Fig. 4, the element corresponding to C2 in Fig. 3); *It should be noted that comparator C2 is analogous to the second buffer circuit.*

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Thörnblad's bidirectional buffer (i.e. Fig. 4) at both ends of AAPA/Chow's ring bus because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing impedance matching between the control device and ring bus so as to protect the control device from destructive voltage transients on the ring bus.

Therefore, it would have been obvious to combine AAPA, Chow, and Thörnblad for the benefit of obtaining the invention as specified in claim 1.

5. Claims 2, 15, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lasker et al. (U.S. Patent 5,586,291) (hereinafter "Lasker").

6. As per claim 2, AAPA discloses a memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data (pg. 2, lines 14-17; Fig. 2, elements 112₁₋₄);

a control device for, in replacing an arbitrary memory module, switching a ring bus from a unidirectional bus capable of either sending or receiving a signal unidirectionally to a bi-directional bus capable of sending and receiving a signal bi-directionally (pg. 2, line 25 – pg. 3, line 5; Fig. 2, element 113); *Please see the citation note for the similar limitation in claim 1 above.*

a CPU which controls said control device for access operation to said memory modules (Fig. 2, element 111),

wherein said buffer sections are connected in series to form the ring bus with said control device, each having a buffer circuit for causing said ring bus to operate as said unidirectional bus or said bi-directional bus in accordance with an instruction from said control device (pg. 2, lines 14-17; pg. 2, line 21 – pg. 3, line 5; Fig. 2).

AAPA admitted prior art does not expressly disclose a hard disk device to which the data stored in said memory modules is copied;

a storage to which data stored in an arbitrary memory module is temporarily copied

a control device for detecting an address space of said memory module to be replaced, copying data corresponding to the detected address space from said hard disk device to said storage, and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested;

and wherein said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus;

a second buffer circuit for sending a signal to one input/output end of the ring bus;

a third buffer circuit for receiving a signal from the other input/output end of the ring bus;

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus.

Lasker discloses a hard disk device to which the data stored in said memory modules is copied (col. 7, line 26; Fig. 1, element 18); *It should noted that "disk drive" is analogous to "hard disk device."*

a storage to which data stored in an arbitrary memory module is temporarily copied (col. 9, lines 42-43; Fig. 2, elements 34a' and 34b'); *It should noted that "NVSIMM 34b'" is analogous to "memory module" and "NVSIMM 34a' " is analogous to "storage."*

a control device for detecting an address space of said memory module to be replaced, copying data corresponding to the detected address space from said hard disk device to said storage, and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested (col. 9, lines 38-48; col. 15, line 66 – col. 16, line 2; Fig. 2, elements 40, 34a', and 34b'; Fig. 6, element 122). *It should be noted that "cache memory control circuit" is analogous to "control device." It should be also be noted that when NVSIMM 34a' is placed into a different controller for the failed NVSIMM 34b' it is inherently required cache memory control circuit detect an address space of NVSIMM 34b', copy data corresponding to the detected address space (i.e. the same data corresponding to the detected address space from said hard disk device) from NVSIMM 34b' to NVSIMM 34a', and then access a memory area in NVSIMM 34a' at the time when an access to NVSIMM 34b' is requested. Finally, it should be noted the*

"DMA transfer between the disk drives and the cache memory of the disk controller" is analogous to "copying data corresponding to the detected address space from said hard disk device to said storage."

AAPA and Lasker are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Lasker's mirror mode modules within AAPA's RAMLINK memory system.

The motivation for doing so would have been to reduce the potential for data loss (Lasker, col. 9, line 49).

The combination of AAPA/Lasker does not expressly disclose said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus;

a second buffer circuit for sending a signal to one input/output end of the ring bus;

a third buffer circuit for receiving a signal from the other input/output end of the ring bus;

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus.

Thörnblad discloses a first buffer circuit for receiving a signal from one input/output end of a bus (col. 3, lines 46-52; Fig. 4, the element corresponding to C1 in Fig. 3); *See the citation note for the similar limitation in claim 1 above.*

a second buffer circuit for sending a signal to one input/output end of the ring bus (col. 3, lines 46-52; Fig. 4, the element corresponding to C2 in Fig. 3); *See the citation note for the similar limitation in claim 1 above.*

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Thörnblad's bidirectional buffer (i.e. Fig. 4) at both ends of AAPA/Lasker's ring bus because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing impedance matching between the control device and ring bus so as to protect the control device from destructive voltage transients on the ring bus.

Therefore, it would have been obvious to combine AAPA, Lasker, and Thörnblad for the benefit of obtaining the invention as specified in claim 2.

7. **As per claim 15**, the combination of AAPA/Lasker/Thörnblad discloses said storage is a memory module for mirroring which is provided with a memory area for holding data and a buffer section for sending and receiving data (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *It should be noted that in order for any data to be written to and copied from the NVSIMM 34a' it is inherently required the NVSIMM 34a' have a some sort of "buffer section."*

8. **As per claim 17**, the combination of AAPA/Lasker/Thörnblad discloses said storage is a memory for graphics (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *It should be noted that this limitation is merely an intended use of the claimed invention. Since Lasker's NVSIMM 34a' is capable of performing the intended use (i.e. capable of being a graphics memory), it therefore meets the claim.*

9. **As per claim 19**, the combination of AAPA/Lasker/Thörnblad discloses said storage is free memory areas of the other memory modules excluding said memory module to be replaced (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *It should be noted that NVSIMM 34b' is the failed memory module to be replaced and the mirrored data is stored on the free area of NVSIMM 34a' (i.e. another memory module which is not the memory module being replaced).*

10. **Claims 5, 8, 16, 18, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lasker and Funaba et al. (U.S. Patent 6,411,539) (hereinafter "Funaba").

11. **As per claim 5**, the combination of AAPA/Lasker discloses a memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data (AAPA, pg. 2, lines 14-17; Fig. 2, elements 112₁₋₄);

a hard disk device to which the data stored in said memory modules is copied (Lasker, col. 7, line 26; Fig. 1, element 18); *Please see the citation note for the similar limitation in claim 2 above.*

a storage to which data stored in an arbitrary memory module is temporarily copied (Lasker, col. 9, lines 42-43; Fig. 2, elements 34a' and 34b'); *Please the citation note for the similar limitation in claim 2 above.*

a control device for, in replacing an arbitrary memory module, detecting an address space of said memory module to be replaced, copying data corresponding to the detected address space from said hard disk device to said storage, and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested (Lasker, col. 9, lines 38-48; col. 15, line 66 – col. 16, line 2; Fig. 2, elements 40, 34a', and 34b'; Fig. 6, element 122); *Please the citation note for the similar limitation in claim 2 above.*

and a CPU which controls said control device for access operation to said memory modules (AAPA, Fig. 2, element 111),

wherein said buffer sections are connected in series to form a unidirectional bus capable of either sending or receiving a signal unidirectionally (pg. 2, lines 25 – pg. 3, line 2; Fig. 2).

Please see the 103 rejection of claim 2 above for the reasons to combine AAPA and Lasker.

The combination of AAPA/Lasker does not expressly disclose a short-circuit device for, in replacing an arbitrary memory module, recovering bus connection which is disconnected by removing said memory module to be replaced;

and wherein said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus;

a second buffer circuit for sending a signal to one input/output end of the ring bus;

a third buffer circuit for receiving a signal from the other input/output end of the ring bus;

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus.

Funaba discloses a short-circuit device for, in replacing an arbitrary memory module, recovering bus connection which is disconnected by removing said memory module to be replaced (col. 21, lines 8-31; Fig. 34; Fig. 35). *It should be noted that "dummy module" is analogous to "short-circuit device."*

The combination of AAPA/Lasker and Funaba are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Funaba's dummy module within AAPA/Lasker's memory module system.

The motivation for doing so would have been to change the memory capacity of the memory system without producing branching in the paths of the signal wirings, thus causing an increase in wiring length (Funaba, col. 21, lines 28-31).

The combination of AAPA/Lasker/Funaba does not expressly disclose said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus;

a second buffer circuit for sending a signal to one input/output end of the ring bus;

a third buffer circuit for receiving a signal from the other input/output end of the ring bus;

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus.

Thörnblad discloses a first buffer circuit for receiving a signal from one input/output end of a bus (col. 3, lines 46-52; Fig. 4, the element corresponding to C1 in Fig. 3); *See the citation note for the similar limitation in claim 1 above.*

a second buffer circuit for sending a signal to one input/output end of the ring bus (col. 3, lines 46-52; Fig. 4, the element corresponding to C2 in Fig. 3); *See the citation note for the similar limitation in claim 1 above.*

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Thörnblad's bidirectional buffer (i.e. Fig. 4) at both ends of AAPA/Lasker/Funaba's ring bus because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing impedance matching between the control device and ring bus so as to protect the control device from destructive voltage transients on the ring bus.

Therefore, it would have been obvious to combine AAPA, Lasker, Funaba, and Thörnblad for the benefit of obtaining the invention as specified in claim 5.

12. **As per claim 8**, the combination of AAPA/Lasker/Funaba/Thörnblad discloses said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module (Funaba, col. 21, lines 8-31; Fig. 34; Fig. 35).

13. **As per claim 16**, the combination of AAPA/Lasker/Funaba/Thörnblad discloses said storage is a memory module for mirroring which is provided with a memory area for holding data and a buffer section for sending and receiving data (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 15 above.*

14. **As per claim 18**, the combination of AAPA/Lasker/Funaba/Thörnblad discloses said storage is a memory for graphics (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 17 above.*

15. **As per claim 20**, the combination of AAPA/Lasker/Funaba/Thörnblad discloses said storage is free memory areas of the other memory modules excluding said memory module to be replaced (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 19 above.*

16. **Claims 3, and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Chow and Thörnblad as applied to claim 1 above, and further in view of Funaba.

17. **As per claim 3**, the combination of AAPA/Chow/Thörnblad discloses all the limitations of claim 3 except a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module.

Funaba discloses a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module (col. 21, lines 8-31; Fig. 34; Fig. 35). *It should be noted that "dummy module" is analogous to "short-circuit device."*

The combination of AAPA/Chow/Thörnblad and Funaba are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Funaba's dummy module within AAPA/Chow/Thörnblad's memory module system.

The motivation for doing so would have been to change the memory capacity of the memory system without producing branching in the paths of the signal wirings, thus causing an increase in wiring length (col. 21, lines 8-31; Fig. 34; Fig. 35).

Therefore, it would have been obvious to combine AAPA/Chow/Thörnblad and Funaba for the benefit of obtaining the invention as specified in claim 3.

18. **As per claim 6**, the combination of AAPA/Lasker/Thörnblad/Funaba discloses said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus

connection which is disconnected by removing said memory module (Funaba, col. 21, lines 8-31; Fig. 34; Fig. 35).

19. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lasker and Thörnblad as applied to claim 2 above, and further in view of Funaba.

20. As per claim 4, the combination of AAPA/Lasker/Thörnblad discloses all the limitations of claim 4 except a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module.

Funaba discloses a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module (col. 21, lines 8-31; Fig. 34; Fig. 35). *It should be noted that "dummy module" is analogous to "short-circuit device."*

Please see the 103 rejection of claim 5 above for the reasons to combine AAPA/Lasker/Thörnblad and Funaba.

21. As per claim 7, the combination of AAPA/Lasker/Thörnblad/Funaba discloses said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module (Funaba, col. 21, lines 8-31; Fig. 34; Fig. 35).

22. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Chow, Thörnblad, and Funaba as applied to claim 3 above, and even further in view of Emerson et al. (U.S. Patent 6,487,623) (hereinafter "Emerson").

23. As per claim 9, the combination of the combination of AAPA/Chow/Thörnblad/Funaba discloses all the limitations of claim 9 except said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module,

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

Emerson discloses said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module (col. 7, lines 12-25; Fig. 4, element 160), *It should be noted "FET signal isolation buffer" is analogous to "FET switch."*

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules (col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *It should be noted that "hot-plug controller" is analogous to "control device."*

It should be noted that the FET isolation buffer's "disconnect" mode is analogous to the "turning ON the FET switch" and conversely the FET isolation buffer's "connect" mode is analogous to "turning OFF the FET switch." The actual states of "ON" and "OFF" are arbitrary and solely dependent on whether a PMOS or NMOS is being used as the FET.

The combination of AAPA/Chow/Thörnblad/Funaba and Emerson are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Emerson's FET isolation buffers and hot-plug controller within AAPA/Chow/Thörnblad/Funaba's memory module system.

The motivation for doing so would have been to easily and safely remove the failing RAM module from its connector without disturbing normal operation of the computer system (Emerson, col. 10, lines 48-51).

Therefore, it would have been obvious to combine AAPA/Chow/Thörnblad/Funaba and Emerson for the benefit of obtaining the invention as specified in claim 9.

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lasker, Thörnblad, and Funaba as applied to claim 4 above, and even further in view of Emerson.

25. As per claim 10, the combination of AAPA/Lasker/Thörnblad/Funaba discloses all the limitations of claim 10 except said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module,

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

Emerson discloses said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module (col. 7, lines 12-25; Fig. 4, element 160), *Please see the citation note for the similar limitation in claim 9 above.*

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules (col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *Please see the citation note for the similar limitation in claim 9 above.*

The combination of AAPA/Lasker/Funaba and Emerson are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Emerson's FET isolation buffers and hot-plug controller within AAPA/Lasker//Thörnblad/Funaba's memory module system.

The motivation for doing so would have been to easily and safely remove the failing RAM module from its connector without disturbing normal operation of the computer system (Emerson, col. 10, lines 48-51).

Therefore, it would have been obvious to combine AAPA/Lasker/Thörnblad/Funaba and Emerson for the benefit of obtaining the invention as specified in claim 10.

26. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lasker, Thörnblad, and Funaba as applied to claim 5 above, and even further in view of Emerson.

27. As per claim 11, the combination of AAPA/Lasker/Thörnblad/Funaba discloses all the limitations of claim 11 except said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module,

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

Emerson discloses said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module (col. 7, lines 12-25; Fig. 4, element 160), *Please see the citation note for the similar limitation in claim 9 above.*

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with

the other memory modules (col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *Please see the citation note for the similar limitation in claim 9 above.*

Please see the 103 rejection of claim 10 above for the reasons to combine AAPA/Lasker/Thörnblad/Funaba and Emerson.

28. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Chow, Thörnblad, and Funaba as applied to claim 3 above, and even further in view of Greeff et al. (U.S. Patent Application Publication 2002/0083255) (hereinafter "Greeff").

29. As per claim 12, the combination of the combination of AAPA/Chow/Thörnblad/Funaba discloses all the limitations of claim 12 except said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

Greeff discloses said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted (paragraph 0069, lines 1-4; Fig. 8, element 55). *It should be noted that "continuity module" is analogous to "connector."*

It should also be noted that at the time a new memory module is inserted it is inherently required the continuity module release the short-circuit.

The combination of AAPA/Chow/Thörnblad/Funaba and Greeff are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Greeff's continuity connector within AAPA/Chow/Thörnblad/Funaba's memory module system.

The motivation for doing so would have been to mitigate bus reflections caused by electrical stubs by connecting contemporaneously-selected system components in a stub-less or substantially stubless configuration using switches, thus improving the performance of a memory bus (Greeff, paragraph 0008, lines 1-6).

Therefore, it would have been obvious to combine AAPA/Chow/Thörnblad/Funaba and Greeff for the benefit of obtaining the invention as specified in claim 12.

30. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lasker, Thörnblad, and Funaba as applied to claim 4 above, and even further in view of Greeff.

31. As per claim 13, the combination of the combination of AAPA/Lasker/Thörnblad/Funaba discloses all the limitations of claim 12 except said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when

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said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

Greeff discloses said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted (paragraph 0069, lines 1-4; Fig. 8, element 55). *Please see the citation note for claim 12 above.*

The combination of AAPA/Lasker/Thörnblad/Funaba and Greeff are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Greeff's continuity connector within AAPA/Lasker/Thörnblad/Funaba's memory module system.

The motivation for doing so would have been to mitigate bus reflections caused by electrical stubs by connecting contemporaneously-selected system components in a stub-less or substantially stubless configuration using switches, thus improving the performance of a memory bus (Greeff, paragraph 0008, lines 1-6).

Therefore, it would have been obvious to combine AAPA/Lasker/Thörnblad/Funaba and Greeff for the benefit of obtaining the invention as specified in claim 13.

32. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lasker, Thörnblad, and Funaba as applied to claims 5 above, and in further view of Emerson.

33. As per claim 14, the combination of the combination of AAPA/Lasker/Thörnblad/Funaba discloses all the limitations of claim 12 except said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

Greeff discloses said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted (paragraph 0069, lines 1-4; Fig. 8, element 55). *Please see the citation note for claim 12 above.*

Please see the 103 rejection of claim 10 above for the reasons to combine AAPA/Lasker/Thörnblad/Funaba and Greeff.

Response to Arguments

34. Applicant's arguments filed in the communication dated August 7, 2007 with respect to **claims 1-20** have been considered but are moot in view of the new grounds

of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

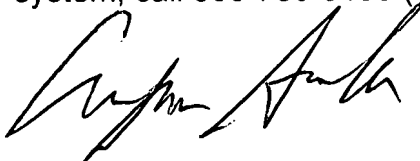
Per the instant office action, **claims 1-20** have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

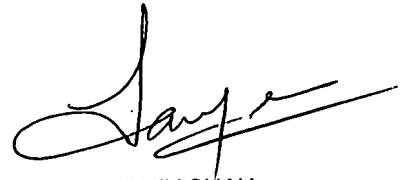
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Arpan Savla
Art Unit 2185
September 17, 2007



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